MULTI-LEVEL CONDUCTIVE LINES WITH REDUCED PITCH

This application is a continuation-in-part of US Patent Application USSN 09/751,492 (Attorney Docket Number 98E9354US), NOW U.S. PATENT No. 6,469,392.

FIELD OF THE INVENTION

The present invention relates to integrated circuits and, more particularly, to integrated circuits with multi-level conductive lines with reduced line pitch.

BACKGROUND OF THE INVENTION

In integrated circuits, parallel conductive lines are widely used to interconnect circuit elements. Fig. 1 shows conductive lines 120 formed on a substrate 101, separated by line spaces 135. The width of the line spacing and conductive line is referred to as the "line pitch". A limiting factor to reducing the line pitch is the minimum resolution or feature size (F) of a specific lithographic tool. With the line spacing and line width equal to 1F each, the minimum line pitch is 2F.

One technique for reducing line pitch below 2F is to provide an additional level 165 on which second conductive lines 125 are formed. By staggering the lines between first and second levels 160 and 165, a line pitch